Power Combining in an Array of Microwave Power Rectifiers

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Abstract—**Microwave power rectifiers have been developed previously with greater than 85-percent RF-to-dc conversion efficiency. To obtain useful power levels for proposed free-space microwave power transmission applications, numerous rectifier outputs are interconnected in series and/or parallel to share a common dc load. This work analyzes the resultant efficiency degradation when identical rectifiers operate at different RF power levels as caused by the power beam taper. Both a closed-form analytical circuit model and a detailed computer-simulation model are used to obtain the output dc load line of the rectifier. The efficiency degradation is nearly identical with series and parallel combining, and the closed-form analytical model provides results which are similar to the detailed computer-simulation model.**

I. Introduction

IN PROPOSED applications of free-space microwave power transmission, large amounts of microwave power must be efficiently converted to dc. To date, highest efficiency of about 90 percent has been achieved with GaAs Schottky rectifiers which are limited to about a 10-W power level. Numerous rectifier circuits, fed from individual receiving elements in a planar array pattern called a "rectenna," share a common dc load to achieve useful power levels. The rectifier outputs can be combined in series and/or parallel to enhance the voltage and/or current levels, respectively [1]–[3].

A fundamental question in this receiving, rectification, and power combining process is caused by the power taper of the incident microwave beam. The incident power density can vary by 10 dB over the rectenna area since a high percentage of the transmitted microwave power usually needs to be collected and the power beam sidelobe level must be kept reasonably low. Since the output (dc terminal) characteristics of the rectifier are power dependent, rectifiers at different power levels that share a common dc load cannot be operated at optimum conditions. With individual rectifiers near 90-percent maximum efficiency, the resultant efficiency degradation can be significant. In this work the efficiency degradation that results when an array of microwave power rectifiers shares a common dc load is evaluated for the first time.

The paper is organized as follows. First, the methodology of the power combining evaluation is presented in general form, followed by the development of special cases of interest with the microwave rectifier. Second, the rectifier equivalent circuit models used in this work are presented. Both an approximate closed-form analytical circuit model and a more exact computer-simulation model are described and compared. Third, the results obtained using these circuit models with the methodology presented originally are given, with some discussion of the impact in proposed applications. Finally the work is summarized. Where applicable, numerical parameters are selected as appropriate for solar power satellites, an application of free-space microwave transmission technology of current interest.

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II. Methodology

In this section we present the method used for determining the loss in power which results when several rectenna elements, operating at different RF power levels, are connected in either series or parallel. The method follows that was developed by Appelbaum *et al.* [4] for determining the maximum power output of an array of nonidentical electrical cells.

We assume that output load line or volt–ampere (V–I) characteristics of each of the rectifying circuits to be combined are known. For the sake of discussion we show in Fig. 1 a general V–I output characteristic of a rectenna element, along with constant power contours. This V–I characteristic can be determined by a circuit analysis of the rectenna element, by a computer simulation, or by direct measurement of the output voltage and current for several load resistances. It is assumed that the V–I characteristics are a function of some parameter θ of the rectenna element (in our case incident RF power). Given the V–I characteristics, it is possible to determine the operating point for maximum power output. For example, if the terminal voltage V is related to the terminal current I by

$$V = f(I,\theta) \tag{1}$$

then the power output is

$$P = IV = If(I,\theta). \tag{2}$$

The current I_m at maximum power P_m is determined from the equation:

$$I_m = -\frac{f(I_m,\theta)}{f'(I_m,\theta)} = \frac{V_m}{r_m} \tag{3}$$

where V_m is the voltage at maximum power and $-r_m$ is the incremental or dynamic resistance at I_m. Notice that the above equation can be written as

$$(R_L)_{op} = r_m \tag{4}$$

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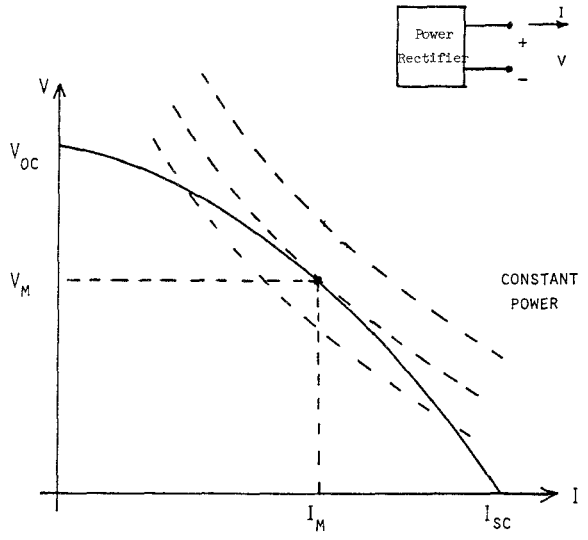

Fig. 1. General V–I characteristics of a power rectifier and optimum operating point.

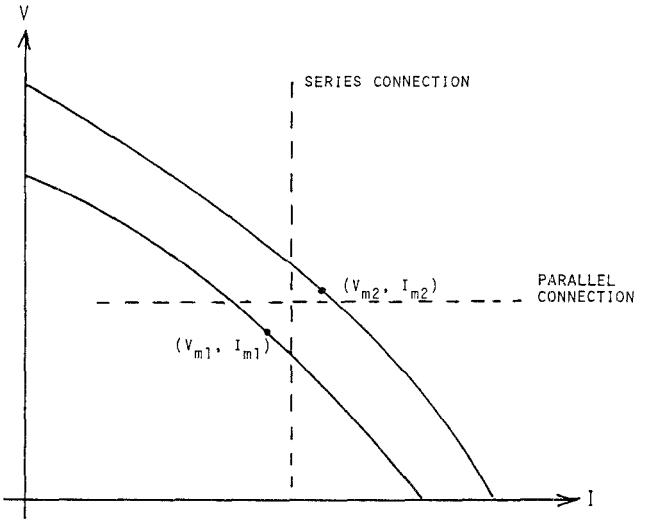

Fig. 2. Series or parallel interconnection of two different rectifiers.

that is, at the optimum power the load resistance is equal to the incremental resistance.

In Fig. 2 we show the V–I characteristics of two dissimilar rectenna elements as well as the points at which each of them deliver maximum power if operating independently. The same figure shows that if the elements are operated in parallel (common output voltage) or in series (common output current), they will not operate at their optimum power output and their combined power output will be less than if operated independently. The difference in the maximum power of N isolated rectenna elements and the maximum power when they are dc interconnected is defined as the power combining loss:

$$(\Delta P)_c = \sum_{j=1}^{N} (P_j)_{\max} - (P_{\max})_c \tag{5}$$

and the ratio:

$$\frac{\Delta P_c}{\sum_{j=1}^{N} (P_j)_{\max}} \tag{6}$$

as the power combining inefficiency.

The maximum power $(P_{\max})_c$ when the several rectenna elements are interconnected can be determined as follows. Let

$$V = f(I, \theta_j), \qquad j = 1, 2, \cdots, N \tag{7}$$

represent the V–I characteristics of each of the N elements. For a series connection, the current I_m and voltage V_m at maximum array power are given by

$$I_m = \frac{\sum_{j=1}^{N} f(I_m, \theta_j)}{\sum_{j=1}^{N} f'(I_m, \theta_j)}$$

$$V_m = \sum_{j=1}^{N} f(I_m, \theta_j) \tag{8}$$

and the array maximum power is

$$(P_{\max})_s = I_m \sum_{j=1}^{N} f(I_m, \theta_j). \tag{9}$$

For a parallel connection, the voltage V_m and current I_m at maximum array power are given by

$$V_m = \frac{\sum_{j=1}^{N} h(V_m, \theta_j)}{\sum_{j=1}^{N} h'(V_m, \theta_j)}$$

$$I_m = \sum_{j=1}^{N} h(V_m, \theta_j) \tag{10}$$

and the array maximum power is

$$(P_{\max})_p = V_m \sum_{j=1}^{N} h(V_m, \theta_j). \tag{11}$$

Equations (8)–(11) are very general and it is desirable to apply them to two particular cases which are of special interest in dealing with arrays of rectenna elements.

First, consider an array of elements in which the V–I characteristics are given by

$$V = V_j - R_j I. \tag{12}$$

That is, the output terminal behavior can be represented by an internal voltage source V_j in series with a resistance R_j, or the load line is linear with both V_j and R_j a function of the RF incident power. As will be shown later, this is an accurate model for the output equivalent circuit of the microwave power rectifier (although a poor model for a solar cell). In the case of an array of series-connected cells, the power combining inefficiency is given by

$$\frac{(\Delta P)_s}{P_{\max}} = \frac{\sum_{j=1}^{N} \frac{V_j^2}{R_j} - \left[\sum_{j=1}^{N} V_j^2\right] \Big/ \sum_{j=1}^{N} R_j}{\sum_{j=1}^{N} \frac{V_j^2}{R_j}} \tag{13}$$

and in the case of parallel connected cells:

$$\frac{(\Delta P)_p}{P_{\max}} = \frac{\sum_{j=1}^{N} \frac{V_j^2}{R_j} - \left(\sum_{j=1}^{N} \frac{1}{R_j}\right)\left(\sum_{j=1}^{N} \frac{V_j}{R_j} \div \sum_{j=1}^{N} \frac{1}{R_j}\right)^2}{\sum_{j=1}^{N} \frac{V_j^2}{R_j}}. \tag{14}$$

A second more restrictive case occurs if all the internal resistances are the same for the rectifiers of the array, which will be shown later to be approximately true for the microwave power rectifier. It can be shown that the power combining inefficiency becomes the same for parallel as well as for series connection, and is given by

$$\frac{\Delta P}{P_{\max}} = 1 - \frac{\left(\sum_{j=1}^{N} V_j\right)^2 / N}{\sum_{j=1}^{N} V_j^2} = 1 - \frac{(V_{\text{av}})^2}{(V^2)_{\text{av}}}. \tag{15}$$

This is an interesting and useful result which is nearly met by the microwave power rectifier, namely that the power combining inefficiency of an array of elements operating at different power levels is nearly independent of the way in which they are interconnected (series or parallel).

III. Microwave Power Rectifier Circuit Models

In order to evaluate the power combining inefficiency with the equations developed previously, an accurate output equivalent circuit model of the conversion circuitry is needed. This was obtained using two independent approaches. Firstly, an approximate closed-form circuit model of the rectifier was developed assuming an ideal diode and lossless circuit elements. The output equivalent circuit was then obtained analytically. Secondly, a more precise computer-simulation model was used, and the output equivalent circuit was obtained by varying the dc load resistance and plotting the resultant output load line. In this section these circuit models are described and the resultant output equivalent circuit models of the rectifier circuitry compared.

While numerous rectifier circuits are possible, a single shunt model diode rectifier circuit has proven most useful in the development work to date [3], and has been assumed in our work. A idealized equivalent circuit of this rectifier is shown in Fig. 3(a), where the filter at the input should prevent any of the dc current and harmonics to flow back through the antenna resistance R_s, but allow current flow at the fundamental RF ω. The function of the filter at the output is not only to prevent ac components to appear across the load terminals but also to allow harmonic currents to flow. In particular, the even harmonics should be allowed to flow since they have the property of having a zero average on each half cycle (harmonics are in phase with respect to fundamental). Therefore, the output filter should allow the even harmonics to flow

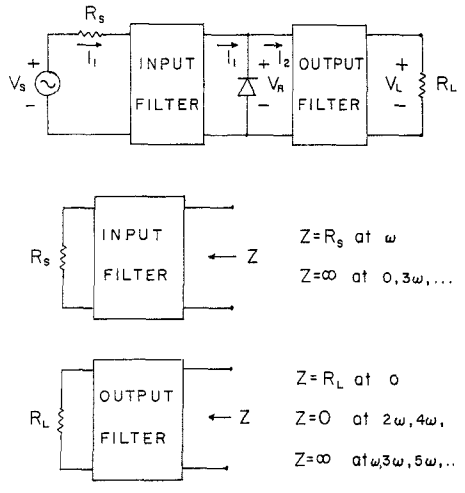

Fig. 3. Rectifier circuit with input and output filters and their frequency characteristics.

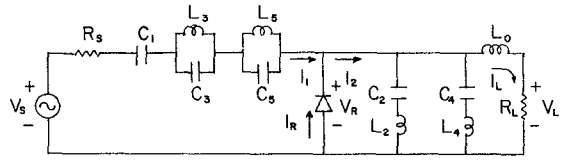

Fig. 4. Realization of a high-efficiency rectifier circuit with lumped-element input and output filters.

without any voltage drop, prevent current flow at any of the odd harmonics, and allow dc current flow. The above characteristics of the input and output filters can be obtained with the impedances shown in Figs. 3(b) and (c), respectively.

We will describe two possible implementations of realizing filters with the above characteristics. Input and output filters implemented using lumped circuit elements and satisfying these requirements are shown in Fig. 4. The elements $L_3, C_3, L_5, C_5, \cdots$, form parallel resonant circuits which are open circuited at the odd harmonics $3\omega, 5\omega, \cdots$, respectively. The capacitor C_1 is used for preventing dc current flow as well as for series resonating $L_3, C_3, L_5, C_5, \cdots$, at the fundamental frequency ω. If that is the case, the current I_1 would be an ac current of fundamental frequency ω. The $L_2, C_2, L_4, C_4, \cdots$, elements in the output circuit are series resonant at the even harmonics $2\omega, 4\omega, \cdots$, respectively. The inductance L_0 is assumed to be large enough such that the current I_L is mainly dc current. In that way the current I_2 would consist of a dc current plus even harmonics only.

Another possible realization of the output filter is shown in Fig. 5. In this circuit the output filter consists of a nondispersive transmission line which is a quarter-wavelength long at the fundamental frequency, terminated in a capacitor C_0 in parallel with the load R_L. If C_0 is sufficiently large, the line can be considered to be shorted at the load end and will appear at the diode terminals as an open circuit at $\omega, 3\omega, 5\omega, \cdots$ and as a short circuit at $2\omega, 4\omega, \cdots$, . The circuit analysis of the rectifiers circuits of Figs. 4 and 5 is identical and is presented below, with

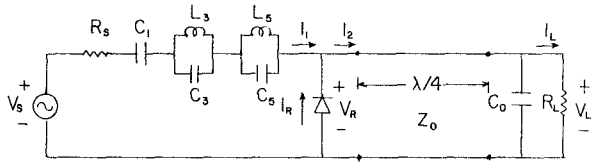

Fig. 5. Realization of a high-efficiency rectifier circuit with a transmission line as output filter.

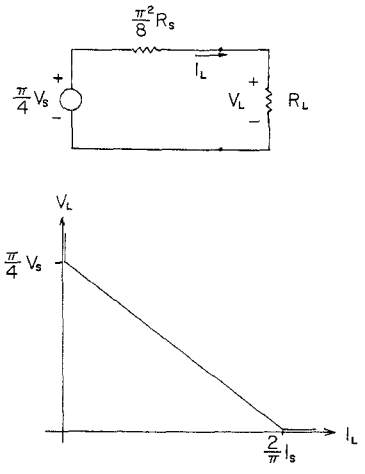

Fig. 6. DC equivalent circuit and load-line characteristics for a high-efficiency closed-form rectifier circuit.

emphasis on obtaining the output load-line characteristics and demonstrating that 100-percent conversion efficiency is indeed obtained with ideal elements.

Since the current $I_1(t)$ in Figs. 3–5 is only of the fundamental frequency and $I_2(t)$ consists only of even harmonics, it follows that [5]

$$V_L = \frac{\pi}{4} V_S - \frac{\pi^2}{8} R_S I_L. \tag{16}$$

The above equation indicates that from the dc load terminals the rectenna elements behaves as a dc voltage source of amplitude $(\pi/4)V_s$ and internal resistance $(\pi^2/8)R_s$. Thus the load shown in Fig. 6 is obtained, except that in the graphical representation we have shown explicitly that $V_L > 0$ and $I_L > 0$ only, as can be seen from Figs. 3–5. Note that the voltage source is power-level dependent, but the equivalent output resistance is independent of RF power.

Using this model, the optimum load for maximum dc load is

$$(R_L)_{\text{op}} = \frac{\pi^2}{8} R_s \tag{17}$$

and the maximum dc power output is

$$(P_L)_{\max} = \frac{\left(\frac{\pi}{8} V_s\right)^2}{\frac{\pi^2}{8} R_s} = \frac{V_s^2}{8R_s} \tag{18}$$

which gives a 100-percent rectification efficiency. This ideal efficiency has been achieved because it was assumed no losses in any of the circuit components or in the diode. However, since these losses can be minimized by choosing a rectifier diode with small forward drop and small-series resistance and high-Q circuit elements, it is expected that the closed-form conversion circuit model would be a good approximation to the characteristics of a high-efficiency rectenna element. Additional factors to be considered are the diode nonlinear depletion layer capacitance and package parasitics. A computer-simulation model is needed to handle these important factors.

In order to evaluate the effect of these additional factors, a detailed computer-simulation model, containing 30 device and circuit parameters and closely representing an actual rectifying circuit, was used. It differs from previously developed computer-simulation models of the rectenna element [6], [7] in that a general circuit program (SPICE 2) [8] is used rather than developing individualized code for the particular circuit. Thus resources needed in development of the model are reduced appreciably, at the expense of less efficient operation for the particular circuit. Attention was focused on obtaining representative efficiency performance, with typical packaged diode characteristics.

The rectifier computer-simulation model is depicted in Fig. 7. Initially we selected reasonable values for the diode parameters and associated mounting parasitic parameters, comparable to that of previously developed rectifiers [3]. Also selected was a 75-Ω antenna resistance, comparable to an isolated $\lambda/2$ dipole receiving element. For simplicity it was decided to keep a 75-Ω RF impedance level throughout the circuit. Although higher efficiency is possible by impedance transforming to a higher value, detailed efficiency optimization was not of main concern. The 2.45-GHz frequency is generally preferred for free-space microwave power transmission applications, particularly for solar power satellites.

With a 75-Ω impedance level selected, a five-stage lumped Chebyshev filter was used at the input and a two-stage smoothing filter at the output. In order to obtain conversion efficiencies above 80 percent, input and output transmission lines were added between the mounted diode and filters. The transmission line controls the phase of reflected signals and is particularly important at the input. In many simulations, a five-section L–C network was used to replace the transmission lines, to reduce program running time without sacrificing accuracy.

With this model, the incident power is varied by changing the value of the amplitude of the voltage source. As a result, the nonlinear circuit performance changes, principally due to the diode turn-on voltage of approximately 0.8 V. A plot of conversion efficiency versus incident power is shown in Fig. 8, in which no circuit or diode parameters have been varied. This decrease in efficiency with decreasing power is greater than experimentally obtained when circuit is reoptimized at each power level [3]. Optimization at each power level was not performed in our work, but we believe that the power combining inefficiency is relatively insensitive to this further optimization.

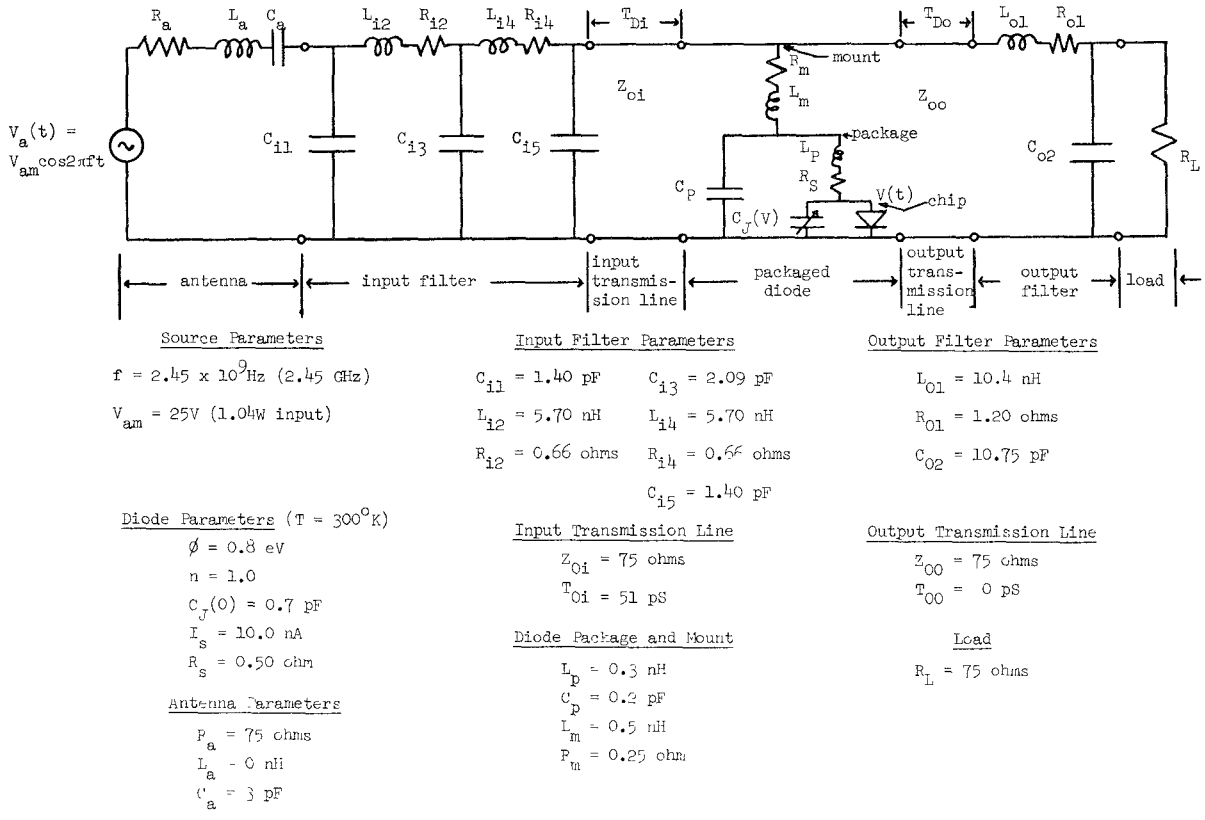

Fig. 7. Computer-simulation model for rectenna RF-to-dc conversion circuitry.

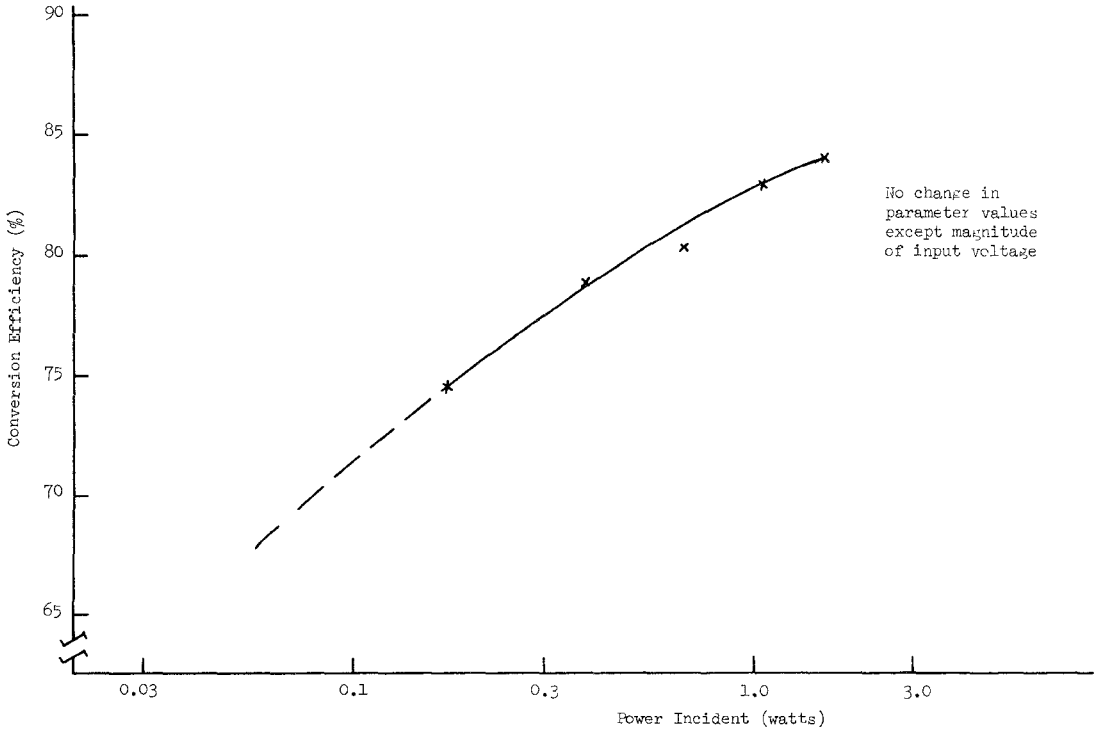

Fig. 8. Conversion efficiency of computer-simulation model

Besides the conversion efficiency one can obtain useful voltage and current waveforms as well as Fourier analysis of these waveforms. It is useful to show that these waveforms are appreciably different than with the idealized analytical model described previously. For example, Figs. 9 and 10 indicate packaged-diode and diode-chip waveforms of voltage and current, respectively, at a 1-W power level. The chip reverse voltage slightly exceeds the peak

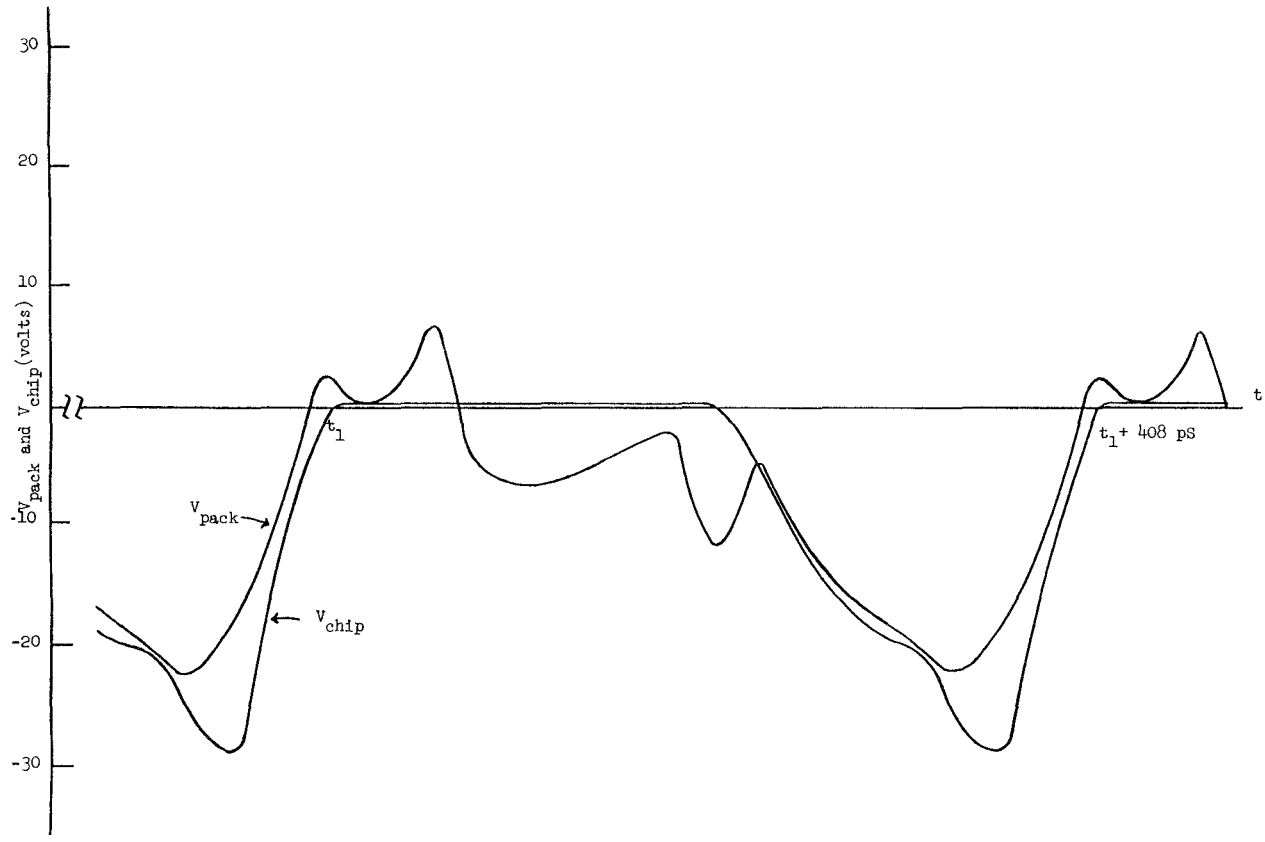

Fig. 9. Package and chip voltage waveforms of computer-simulation model at 1-W level.

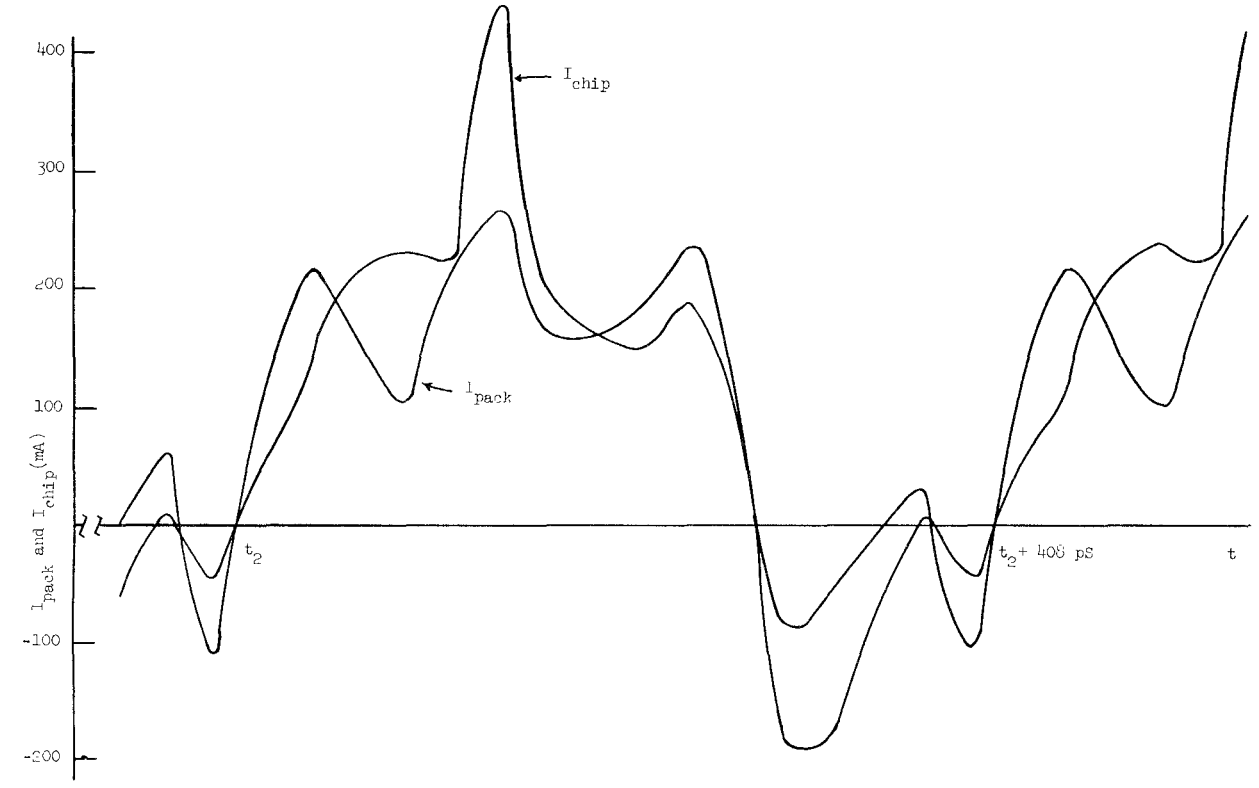

Fig. 10. Package and chip current waveforms (including chip displacement current) of computer-simulation model at 1-W level.

voltage amplitude of the source (29 V compared to peak amplitude of the open-circuited RF source voltage of 25 V) while the chip current (conduction plus displacement) exceeds 400 mA during the middle of the 180° conduction angle (compared to peak amplitude of the short-circuited RF source current of 333 mA). The wave-

TABLE I
COMPUTER SIMULATION OUTPUT FOR CIRCUIT OF FIG. 7 (POWER IN = 1.04 W)

Fourier Components of Transient Response of Output Voltage - DC Component = -8.052D 00 (volts)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	4.971D-01	1.000000	-114.908	0.000
2	4.900D 09	5.658D-02	0.113826	9.055	123.963
3	7.350D 09	1.147D-02	0.023079	61.376	176.284
4	9.800D 09	3.714D-03	0.007472	-15.882	99.026
5	1.225D 10	2.125D-03	0.004274	-47.665	67.243
6	1.470D 10	2.115D-03	0.004255	23.977	138.886
7	1.715D 10	2.603D-03	0.005237	2.376	117.285
8	1.960D 10	6.438D-04	0.001295	14.474	129.382
9	2.205D 10	7.756D-04	0.001560	23.437	138.346

Fourier Components of Transient Response of Mounted Package Voltage - DC Component = -8.194D 00

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized (volts) Phase (Deg)
1	2.450D 09	1.279D 01	1.000000	59.228	0.000
2	4.900D 09	5.672D 00	0.443533	-173.104	-232.332
3	7.350D 09	2.533D 00	0.198123	-112.479	-171.707
4	9.800D 09	1.075D 00	0.084099	152.082	92.854
5	1.225D 10	1.162D 00	0.090878	101.244	42.015
6	1.470D 10	1.233D 00	0.096399	-147.130	-206.359
7	1.715D 10	2.458D 00	0.192248	177.288	118.059
8	1.960D 10	4.572D-02	0.003575	-11.400	-70.628
9	2.205D 10	4.473D-01	0.034980	-131.388	-190.616

Fourier Components of Transient Response of Chip Voltage - DC Component = -8.269D 00 (volts)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	1.396D 01	1.000000	51.526	0.000
2	4.900D 09	6.437D 00	0.460942	-173.499	-225.025
3	7.350D 09	1.623D 00	0.116224	-112.665	-164.191
4	9.800D 09	2.693D 00	0.192868	-27.354	-78.881
5	1.225D 10	1.749D 00	0.125243	100.730	49.204
6	1.470D 10	7.460D-01	0.053421	-145.123	-196.649
7	1.715D 10	4.952D-01	0.035461	-5.913	-57.440
8	1.960D 10	3.836D-01	0.027469	159.988	108.462
9	2.205D 10	1.350D-01	0.009670	-119.313	-170.839

Fourier Components of Transient Response Source Current - DC Component = -1.318D-04 (Amps)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	1.588D-01	1.000000	179.679	0.000
2	4.900D 09	4.186D-04	0.002635	33.824	-145.856
3	7.350D 09	1.699D-05	0.000107	74.036	-105.643
4	9.800D 09	1.084D-05	0.000068	-12.489	-192.168
5	1.225D 10	4.711D-06	0.000030	107.372	-72.307
6	1.470D 10	9.712D-07	0.000006	5.270	-174.410
7	1.715D 10	4.553D-06	0.000029	-68.767	-248.446
8	1.960D 10	7.651D-07	0.000005	174.106	-5.573
9	2.205D 10	4.034D-06	0.000025	77.587	-102.093

forms are obviously rich in harmonic content, partly attributed to resonances from packaged diode parasitics.

Fourier analysis of three voltage waveforms, namely the output voltage, the diode package voltage, and the diode chip voltage are presented in Table I, along with the input current. The effectiveness of the smoothing filter is apparent as the dc voltage is similar while the fundamental voltage is reduced by a factor of 26 (12.79 V–0.497 V) or 28 dB, with harmonics reduced still further (e.g., second harmonic 40 dB). Also the three values of dc voltage are slightly different, due to numerical approximations in the program and finite program running time. These approximations, as well as the effect of the input filter, can be seen from the input current, which contains harmonics 50 dB below the fundamental. This is about the precision of the program as used by us, as can be seen by the erroneous finite value of dc input current (should be zero). As a result of these and similar considerations, we concluded that the computer-simulation model developed results in performance characteristics similar to the actual power rectifiers developed to date.

Output load-line characteristics were obtained at various power levels by varying the load resistance, and plotting the resultant output dc load-line characteristics. The load line for the computer-simulation model of Fig. 6 obtained by only varying the output load resistance from 5 to 1500 Ω (instead of fixed at 75 Ω) is shown in Fig. 11. As required the computer model load line lies to the left of the closed-form model since the latter does not contain any dissipative loss elements and is 100 percent efficient. Note that the computer model also results in a highly linear load line with similar characteristics to the closed-form model. For convenience, we find it useful to plot a normalized load line, i.e., $V_L/V_S - I_L/I_S$, where V_S is the open-circuited source voltage and I_S is the short-circuited source current.

With the computer-simulation model a normalized load line is not identical at all power levels because of the fixed diode forward drop. The difference is shown in Fig. 12 for a 13-dB power range (0.10–2.08 W). As expected the efficiency increases with increasing power level and the dc output resistance varies only slightly with power level.

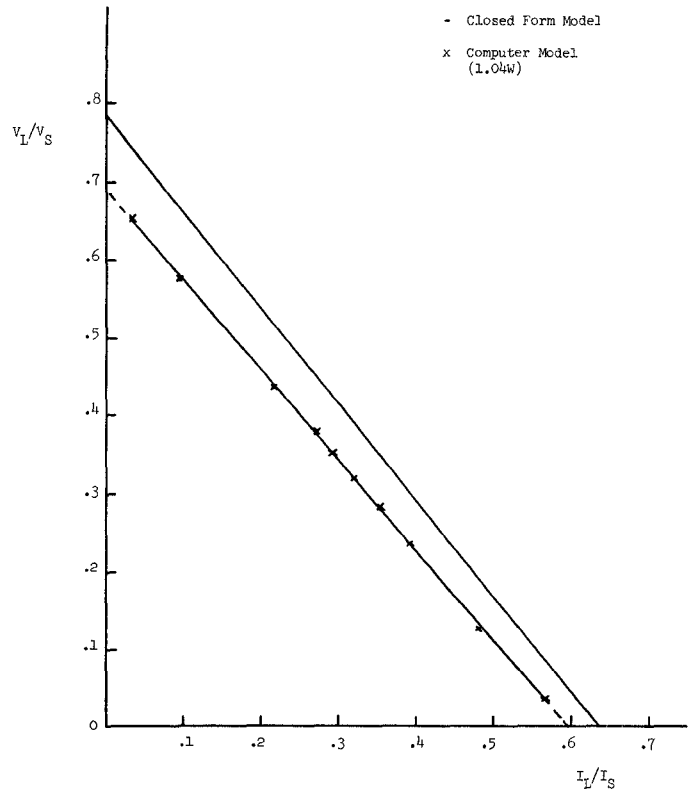

Fig. 11. Normalized load line of closed-form model and computer-simulation model at 1.04 W.

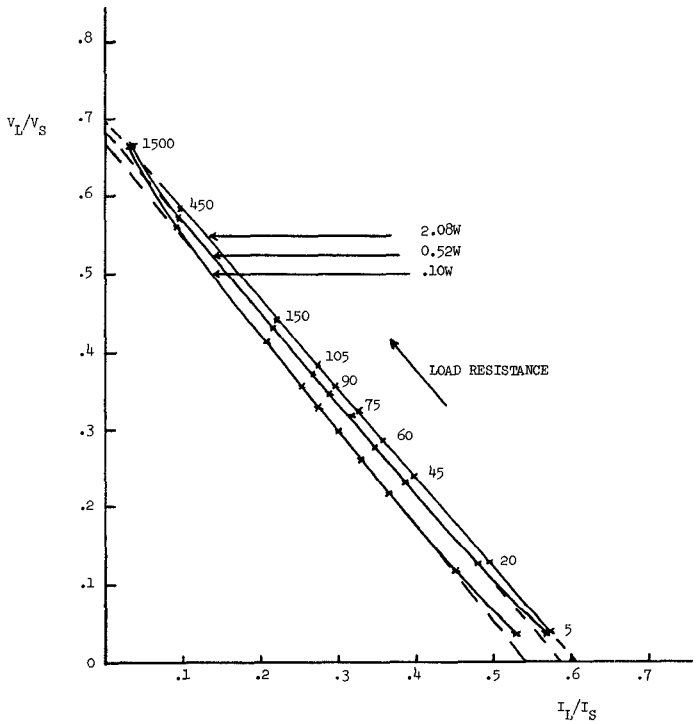

Fig. 12. Normalized load line of computer-simulation model as a function of incident power.

This dependence of output open-circuited voltage V and output equivalent source resistance R on input power level is depicted in Fig. 13, in which the expanded scale should be noted. For comparison purposes the closed-form model described earlier has V/V_S equal to 0.785 and $R/R_S = 1.234$, which is closer to the computer-simulation model results at higher and lower incident power, respectively. Note particularly the normalized output

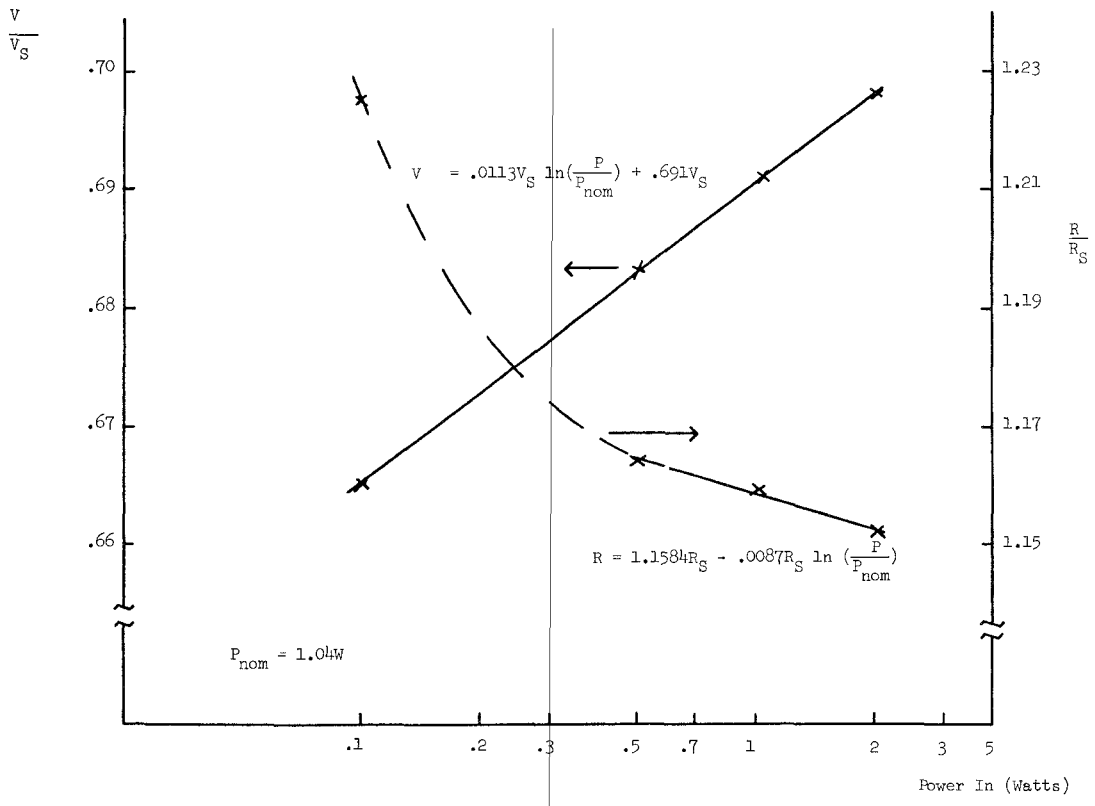

Fig. 13. Output equivalent circuit parameters of computer-simulation model as a function of incident power.

TABLE II
TYPICAL POWER DISTRIBUTIONS (DISCRETE PROBABILITY DENSITY FUNCTIONS) WITH RESULTANT POWER COMBINING INEFFICIENCY USING COMPUTER-SIMULATION MODEL AND CLOSED-FORM MODEL

	$\frac{P}{P_{nom}}$ where $P_{nom} = 1.04W$															
	.5	.6	.7	.8	.9	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
Relative Number																
Case 1	.1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.9
Case 2	.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.5
Case 3	.9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.1
Case 4	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{15}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$
Case 5	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	-	-	-	-	-	-

	Computer Simulation Model		Closed Form Model
	Series Combining	Parallel Combining	(Series and Parallel)
Case 1	2.61	2.52	2.43
Case 2	10.83	10.51	10.00
Case 3	7.68	7.51	6.92
Case 4	3.98	3.87	3.67
Case 5	2.62	2.55	2.40

parameters V/V_S and R/R_S are relatively insensitive to input power.

IV. Power Combining Inefficiency Results

A number of cases were calculated to arrive at a comparison between parallel and series power combining inefficiency with the computer simulation model and to evaluate the usefulness of the closed-form analytical model. In performing these calculations, discrete probability densities were used with 16 categories of input power ranging from 0.52 to 2.08 W ($0.5 \leqslant P/P_{nom} \leqslant 2.0$) in approximately 0.1 W steps. The power range was chosen to

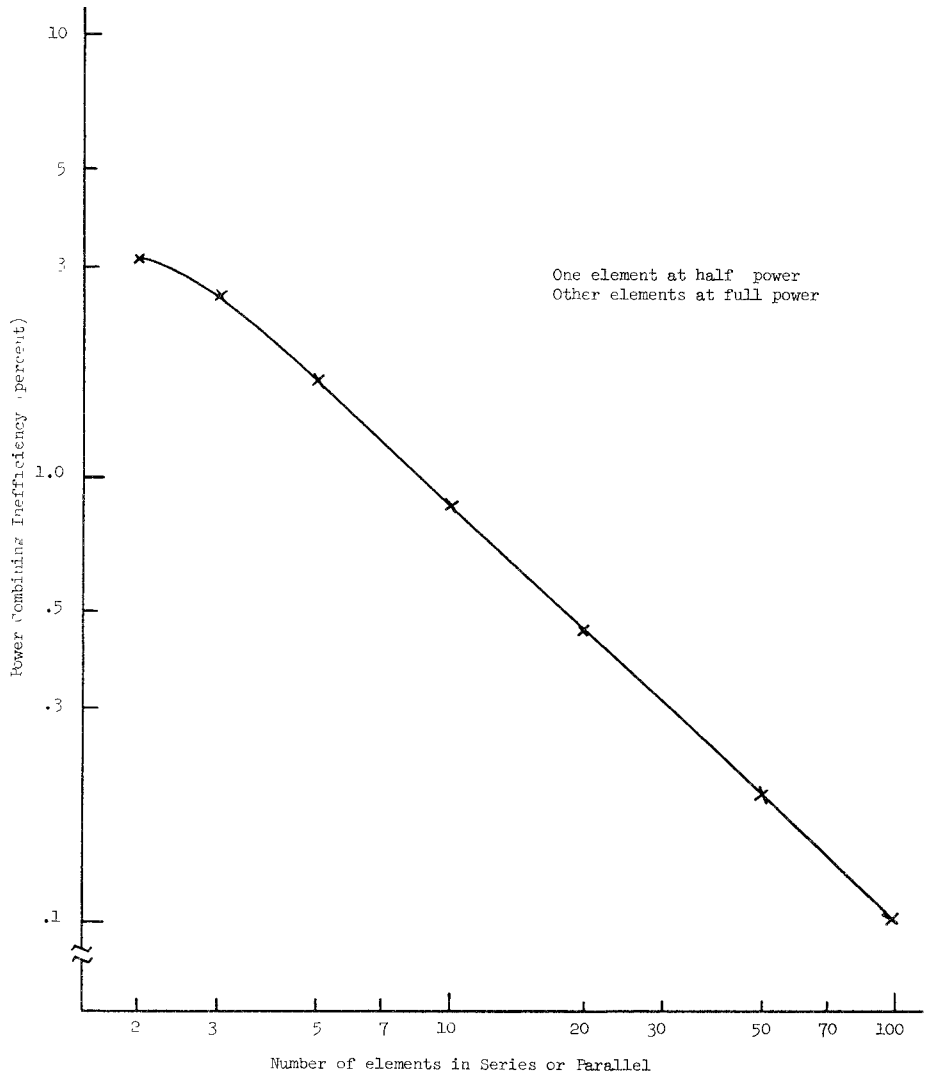

Fig. 14. Power combining inefficiency versus number of elements combined with one element at half power and others at full power.

be comparable to the majority of rectenna elements in proposed solar power satellite (SPS) applications. With the computer-simulation model, the output equivalent circuit parameters were obtained at each power level using the functional form of the expression given in Fig. 13. Naturally the evaluation is simplified with the closed-form model since the output resistance and normalized output open-circuited voltage are independent of power.

Five cases presented for illustrative purposes are shown in Table II. The first three cases are useful in evaluating diffraction effects with a serrated rectenna [7], while the latter two are appropriate for evaluating power beam taper effects. A firm conclusion is that parallel and series power combining inefficiencies are nearly identical, and that the closed-form model underestimates the power loss due to operation into a common load only slightly (by $\sim$10 percent of the power combining inefficiency). The latter two cases shown indicate that the power combining inefficiency at the edge of a rectenna due to the incident power beam taper can be very significant.

The effect of only one element operating at half power in a string of N total elements, $N-1$ operating at full power is shown in Fig. 14. Thus if 10 percent of the elements in a string are at half power, a power combining inefficiency of 1.0 percent would occur, which drops to 0.1 percent if only 1 percent of the elements are operating at half power. The small difference between series and parallel combining cannot be clearly presented on the scale shown.

The effect of the dynamic range of power variation, assuming a uniform power distribution over the dynamic range, is shown in Fig. 15. With a 2-to-1 power range, a 1-percent power combining inefficiency is expected, raising rapidly to over 2.5 percent with a 3-to-1 power range. This curve can influence the dc combining buss design in rectennas for microwave power transmission systems, particularly at the edge of the rectenna where the power beam taper is largest.

While many other cases could be included, these results indicate that the power combining inefficiency can be a serious concern, particularly as the optimum conversion circuitry efficiency exceeds 85 percent. Two particularly significant conclusions are derived from these cases. 1) There is little difference in power combining inefficiency with series and parallel combining for the microwave power rectifier. 2) The closed-form model results

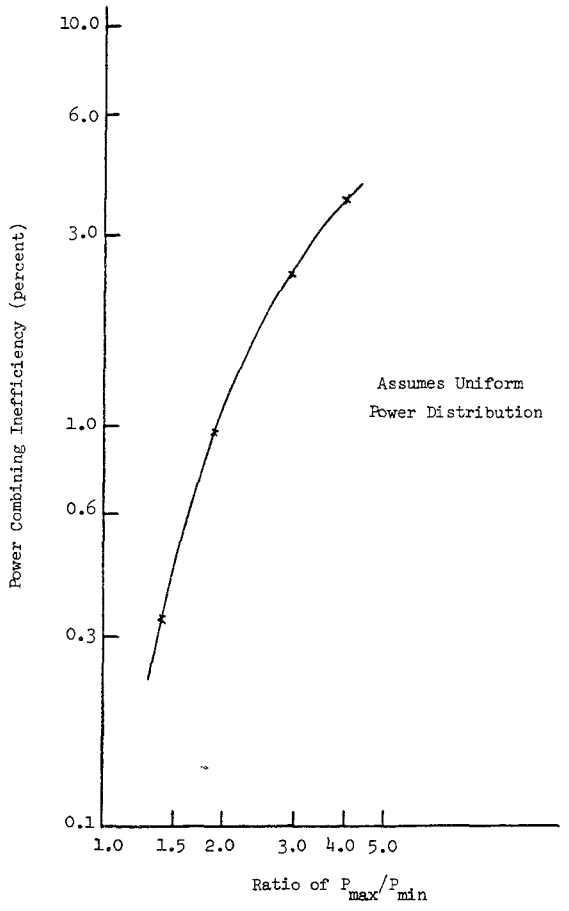

Fig. 15. Power combining inefficiency versus power range (ratio of P_{max}/P_{min}) assuming uniform power distribution.

are extremely useful in evaluation of power combining inefficiency due to incident RF power differences.

V. Summary

In this paper the efficiency degradation that results when an array of microwave power rectifiers shares a common dc load is presented. This efficiency degradation is quite insensitive to the details of the conversion circuitry with highly efficient rectifiers, as indicated by the close numerical agreement using the closed-form analytical model and the detailed computer-simulation model. Unlike with photovoltaics, there is little difference between series and parallel dc combining, as the output load-line characteristic of the microwave power rectifier is quite linear. While not considered in this work, the methodology can be extended to other parameter variations besides power level, for example, diode depletion layer capacitance, in evaluating the efficiency degradation dependence upon diode and circuit parameter tolerances.

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